This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Original) A heterostructure bipolar transistor, comprising:

a substrate comprised of a first semiconductor material doped with impurities of a first type, the substrate including a first conducting region;

a heterostructure alloy region positioned in the substrate and comprised of a heterostructure alloy of atoms of the first semiconductor material and atoms of a second semiconductor material;

a base region positioned in the substrate above the first conducting region and doped with impurities of a second type;

a first dielectric layer positioned on the substrate, the first dielectric layer defining a first window directly above the heterostructure alloy region;

a second conducting region positioned in the heterostructure alloy region and between the first window and the base region, the second conducting region being comprised of the heterostructure alloy doped with impurities of the first type; and

a contact region positioned in the first window and comprised of the first semiconductor material, the contact region directly contacting the heterostructure alloy of the second conducting region in the heterostructure alloy region.

2. (Original) The transistor of claim 1 wherein the first dielectric layer directly contacts the heterostructure alloy of the of the heterostructure alloy region.

3. (Original) The transistor of claim 1, further comprising:

a protective layer positioned over the semiconductor substrate and defining a second window above the heterostructure alloy region, the first dielectric layer being positioned in the second window between the protective layer and the first window.

4. (Original) The transistor of claim 3, further comprising a second dielectric layer positioned on the first dielectric layer and in the second window between the protective layer and the first window.

5. (Original) The transistor of claim 4 wherein the first dielectric layer is silicon dioxide and the second dielectric layer is silicon nitride.

6. (Original) The transistor of claim 1 wherein the first semiconductor material is silicon, the second semiconductor material is germanium.

7. (Original) The transistor of claim 1, further comprising a metal contact formed directly on the contact region.

8. (Original) A heterostructure bipolar transistor, comprising:

a substrate comprised of a first semiconductor material doped with impurities of a first type, the substrate including a first conducting region;

a heterostructure alloy region positioned in the substrate and comprised of a heterostructure alloy of atoms of the first semiconductor material and atoms of a second semiconductor material;

a base region positioned in the substrate above the first conducting region and doped with impurities of a second type;

a first dielectric layer positioned on, and directly contacting, the heterostructure alloy region, the first dielectric layer defining a first window directly above the heterostructure alloy region; and

a second conducting region positioned in the heterostructure alloy region and between the first window and the base region, the second conducting region being comprised of the heterostructure alloy doped with impurities of the first type and directly contacting the first dielectric layer.

9. (Original) The transistor of claim 8, further comprising:

a protective layer positioned over the semiconductor substrate and defining a second window above the heterostructure alloy region, the first dielectric layer being positioned in the second window between the protective layer and the first window.

10. (Original) The transistor of claim 9, further comprising a second dielectric layer positioned on the first dielectric layer and in the second window between the protective layer and the first window.

11. (Original) The transistor of claim 10 wherein the first dielectric layer is silicon dioxide and the second dielectric layer is silicon nitride.

12. (Original) The transistor of claim 8 wherein the first semiconductor material is silicon, the second semiconductor material is germanium.

13. (Original) The transistor of claim 8, further comprising:

a contact region positioned in the first window and comprised of the first semiconductor material, the contact region directly contacting the heterostructure alloy of the second conducting region in the heterostructure alloy region; and

a metal contact formed directly on the contact region.

14. (Previously Presented) A vertical structure high carrier mobility bipolar transistor, comprising a substrate of crystalline silicon doped with impurities of the N type, having a collector region located at a lower portion of the substrate, the transistor being obtained by a process that includes:

defining a window above the substrate;

providing a first implantation of germanium atoms through said window into the substrate;

providing a second implantation of acceptor dopants through said window to define a base region in the substrate;

applying an RTA treatment, or treatment in an oven, to re-construct a crystal lattice within the semiconductor substrate comprising a silicon/germanium alloy;

forming by chemical vapor deposition a first thin dielectric layer of silicon dioxide on the substrate;

depositing a second dielectric layer onto said first dielectric layer;

depositing a polysilicon layer onto said second dielectric layer;

etching away, within the window region, said first and second dielectric layers, and the polysilicon layer, to expose the base region and form isolation spacers at edges of the window; and

forming an N-doped emitter in the base and window regions.

15. (Original) The transistor of claim 14 wherein the deposition of the first thin dielectric layer of silicon dioxide is carried out by an atmospheric pressure chemical vapor deposition process.

16. (Original) The transistor of claim 14 wherein the deposition of the first thin dielectric layer of silicon dioxide is followed by thermal treatment.

17. (Original) The transistor of claim 14 wherein the second dielectric layer is silicon nitride.

18. (Original) The transistor of claim 14 wherein the emitter directly contacts the first dielectric layer.